



H67H2-M3

Rev : 1.0

ECS CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
V.A	2010/05/20	Change from H67H2-M: 1. audio change to alc662/vt1705 2. 4*dimm change to 2*dimm 3. rear IO(PS2/HDMI co-lay DVI) 4. Super IO change to IT8758E
V.B	2010/08/10	Change from V.A: 1. Vcore co-lay RT8859M/Layout change VR12 ref GND 2. GP_V1.05 change to PCH 3. USB3.0 IC co-lay 3VSB 4. PCH change to QS 5. IT8893/EJ168 use Version:B 6. Add EZ charger circuit 7. BIOS ROM change to 32M
V.1.0	2010/10/11	Change from V.B: 1. EJ168 SMI to PCH for dos mode 2. power change as vendor 3. change IT8893 to CX 4. change HDMI ddc clk/data ESD to ESD-6P 5. Audio co-lay VT1705CE 6. change EN_6536 control for support decrease V_DIMM 7. change 25M cap to 22P for RTC

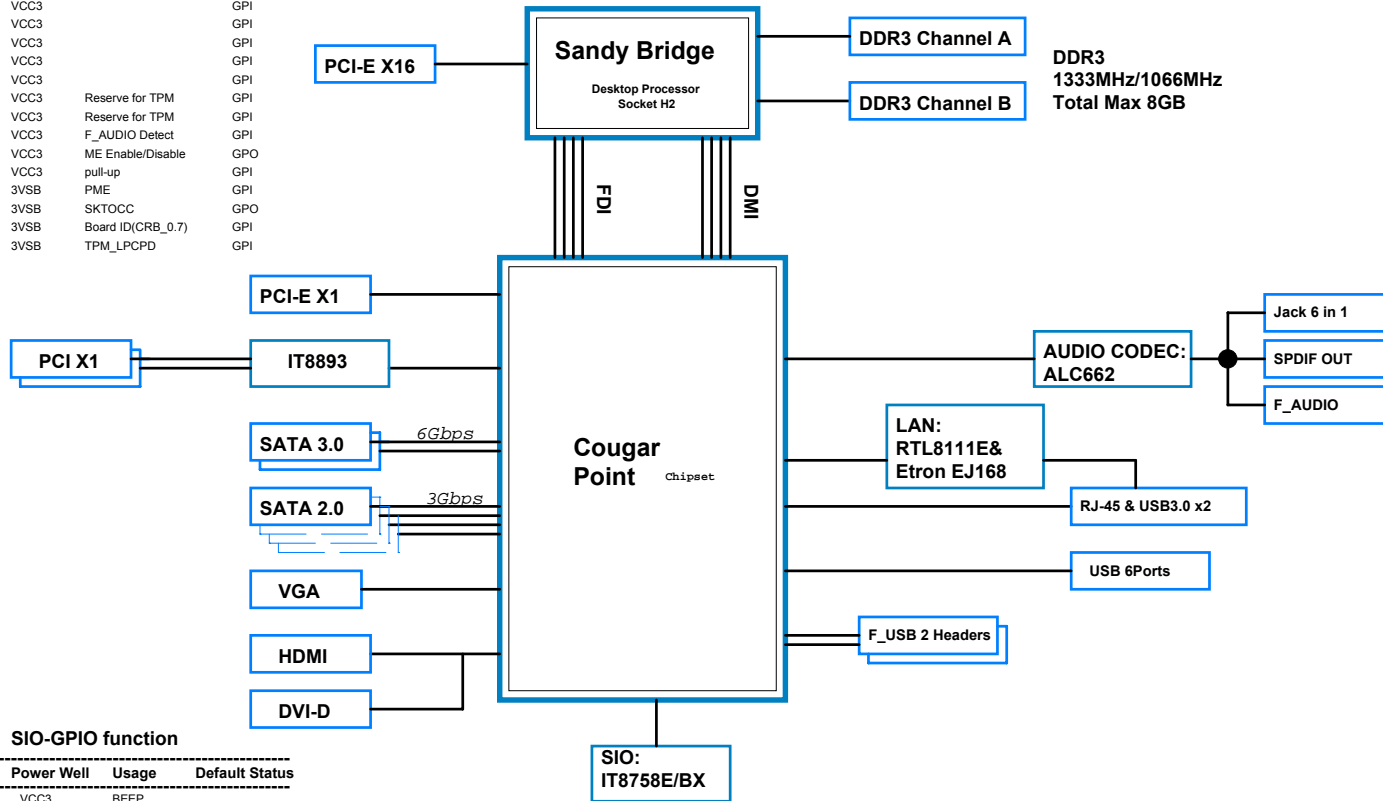
NOTE:

Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev_0_8.pdf,
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		Elitegroup Computer Systems	
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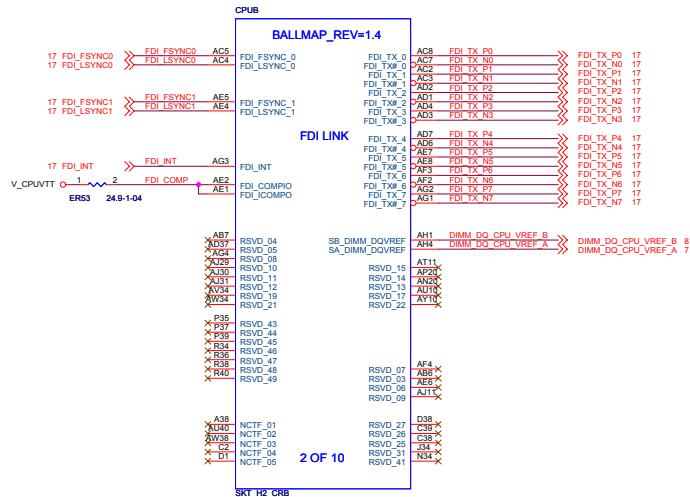
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPI071	VCC3		GPI
GPI022	VCC3		GPI
GPI038	VCC3		GPI
GPI039	VCC3		GPI
GPI048	VCC3		GPI
GPI021	VCC3		GPI
GPI036	VCC3		GPI
GPI037	VCC3		GPI
GPI016	VCC3	Reserve for TPM	GPI
GPI049	VCC3	Reserve for TPM	GPI
GPI00	VCC3	F_AUDIO Detect	GPI
GPI033	VCC3	ME Enable/Disable	GPO
GPI034	VCC3	pull-up	GPI
GPI013	3VSB	PME	GPI
GPI024	3VSB	SKTOCC	GPO
GPI057	3VSB	Board ID(CRB_0.7)	GPI
GPI061	3VSB	TPM_LPCPD	GPI



SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	



These signals are available for Workstation only

These signals are available for Workstation only

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SKT H2 CRE

01D201-000060 PCH ESO

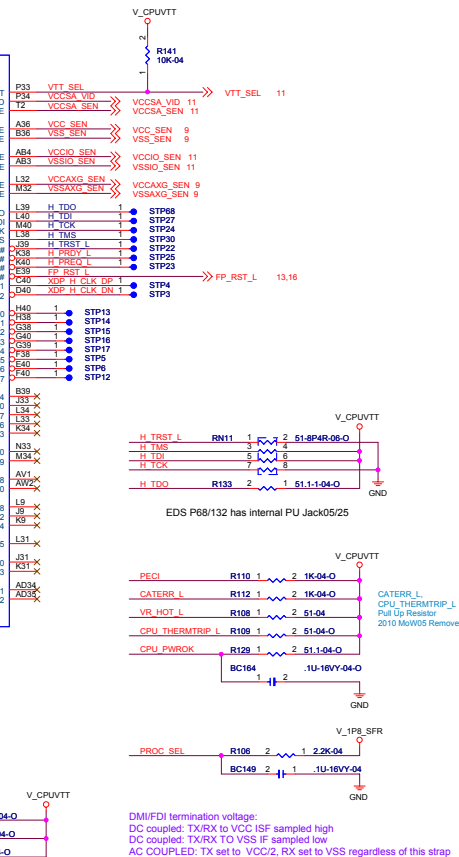
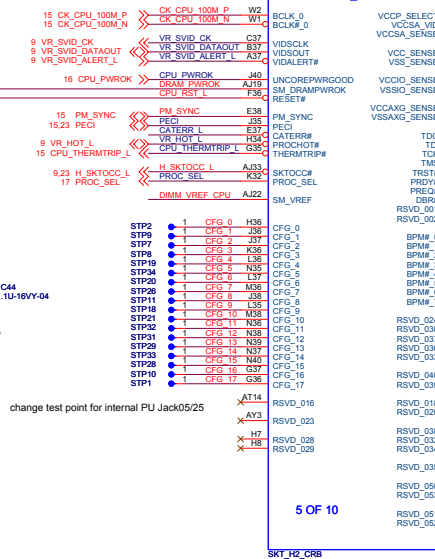
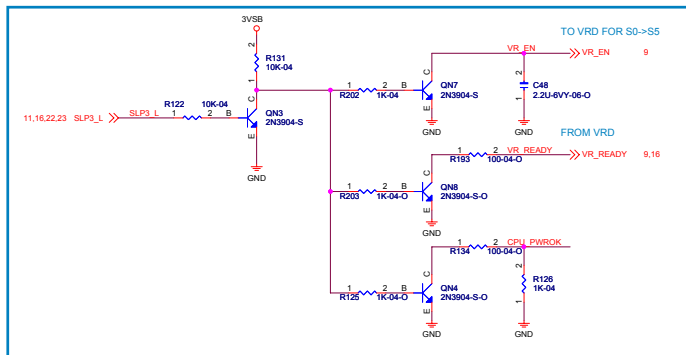
11-018-115021 CPU SMD SOCKET
SOCKET.CPU_LGA 1155P SMD.BLACK.PE115527-4041-01F.
LEAD-FREE.FOXCONN

20-800-004711 CPU SOCKET STEEL
SUBASSY,STEEL LGA 1156P.W/
BACK PLATE PT44A11-6401,LEAD-FREE(RoHS),FOXCONN

CFG [0..17] HAVE INTERNAL PULL-UPS

CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8 X4 X4

Power Down Sequencing Circuit



7 M_DATA_A0_63] << M_DATA_A0_63
 7 M_DQS_A_P0_7] << M_DQS_A_P0_7
 7 M_DQS_A_N0_7] << M_DQS_A_N0_7
 7 M_MA_A0_15] << M_MA_A0_15
 7 M_BS_A0_2] << M_BS_A0_2
 7 M_CS_A_L0_1] << M_CS_A_L0_1
 7 M_CKE_A0_1] << M_CKE_A0_1
 7 M_ODT_A0_1] << M_ODT_A0_1
 7 M_CLK_A_P0_1] << M_CLK_A_P0_1
 7 M_CLK_A_N0_1] << M_CLK_A_N0_1

DDR3 CH.A

7.8 DDR3_DRAMRST_L << DDR3_DRAMRST_L

8 M_DATA_B0_63] << M_DATA_B0_63
 8 M_DQS_B_P0_7] << M_DQS_B_P0_7
 8 M_DQS_B_N0_7] << M_DQS_B_N0_7
 8 M_MA_B0_15] << M_MA_B0_15
 8 M_BS_B0_2] << M_BS_B0_2
 8 M_CS_B_L0_1] << M_CS_B_L0_1
 8 M_CKE_B0_1] << M_CKE_B0_1
 8 M_ODT_B0_1] << M_ODT_B0_1
 8 M_CLK_B_P0_1] << M_CLK_B_P0_1
 8 M_CLK_B_N0_1] << M_CLK_B_N0_1

DDR3 CH.B

8 M_WE_B_L << M_WE_B_L
 8 M_CAS_B_L << M_CAS_B_L
 8 M_RAS_B_L << M_RAS_B_L

M_DATA_A0_AJ3 SA_DQ_0
 M_DATA_A1_AJ4 SA_DQ_1
 M_DATA_A2_AJ5 SA_DQ_2
 M_DATA_A3_AJ6 SA_DQ_3
 M_DATA_A4_AJ7 SA_DQ_4
 M_DATA_A5_AJ8 SA_DQ_5
 M_DATA_A6_AJ9 SA_DQ_6
 M_DATA_A7_AJ0 SA_DQ_7
 M_DATA_A8_AJ1 SA_DQ_8
 M_DATA_A9_AJ2 SA_DQ_9
 M_DATA_A10_AJ3 SA_DQ_10
 M_DATA_A11_AJ4 SA_DQ_11
 M_DATA_A12_AJ5 SA_DQ_12
 M_DATA_A13_AJ6 SA_DQ_13
 M_DATA_A14_AJ7 SA_DQ_14
 M_DATA_A15_AJ8 SA_DQ_15
 M_DATA_A16_AJ9 SA_DQ_16
 M_DATA_A17_AJ0 SA_DQ_17
 M_DATA_A18_AJ1 SA_DQ_18
 M_DATA_A19_AJ2 SA_DQ_19
 M_DATA_A20_AJ3 SA_DQ_20
 M_DATA_A21_AJ4 SA_DQ_21
 M_DATA_A22_AJ5 SA_DQ_22
 M_DATA_A23_AJ6 SA_DQ_23
 M_DATA_A24_AJ7 SA_DQ_24
 M_DATA_A25_AJ8 SA_DQ_25
 M_DATA_A26_AJ9 SA_DQ_26
 M_DATA_A27_AJ0 SA_DQ_27
 M_DATA_A28_AJ1 SA_DQ_28
 M_DATA_A29_AJ2 SA_DQ_29
 M_DATA_A30_AJ3 SA_DQ_30
 M_DATA_A31_AJ4 SA_DQ_31
 M_DATA_A32_AJ5 SA_DQ_32
 M_DATA_A33_AJ6 SA_DQ_33
 M_DATA_A34_AJ7 SA_DQ_34
 M_DATA_A35_AJ8 SA_DQ_35
 M_DATA_A36_AJ9 SA_DQ_36
 M_DATA_A37_AJ0 SA_DQ_37
 M_DATA_A38_AJ1 SA_DQ_38
 M_DATA_A39_AJ2 SA_DQ_39
 M_DATA_A40_AJ3 SA_DQ_40
 M_DATA_A41_AJ4 SA_DQ_41
 M_DATA_A42_AJ5 SA_DQ_42
 M_DATA_A43_AJ6 SA_DQ_43
 M_DATA_A44_AJ7 SA_DQ_44
 M_DATA_A45_AJ8 SA_DQ_45
 M_DATA_A46_AJ9 SA_DQ_46
 M_DATA_A47_AJ0 SA_DQ_47
 M_DATA_A48_AJ1 SA_DQ_48
 M_DATA_A49_AJ2 SA_DQ_49
 M_DATA_A50_AJ3 SA_DQ_50
 M_DATA_A51_AJ4 SA_DQ_51
 M_DATA_A52_AJ5 SA_DQ_52
 M_DATA_A53_AJ6 SA_DQ_53
 M_DATA_A54_AJ7 SA_DQ_54
 M_DATA_A55_AJ8 SA_DQ_55
 M_DATA_A56_AJ9 SA_DQ_56
 M_DATA_A57_AJ0 SA_DQ_57
 M_DATA_A58_AJ1 SA_DQ_58
 M_DATA_A59_AJ2 SA_DQ_59
 M_DATA_A60_AJ3 SA_DQ_60
 M_DATA_A61_AJ4 SA_DQ_61
 M_DATA_A62_AJ5 SA_DQ_62
 M_DATA_A63_AJ6 SA_DQ_63

M_DQS_A_P0_AK3 SA_DQS_0
 M_DQS_A_P1_AK4 SA_DQS_1
 M_DQS_A_P2_AK5 SA_DQS_2
 M_DQS_A_P3_AK6 SA_DQS_3
 M_DQS_A_P4_AK7 SA_DQS_4
 M_DQS_A_P5_AK8 SA_DQS_5
 M_DQS_A_P6_AK9 SA_DQS_6
 M_DQS_A_P7_AK0 SA_DQS_7

M_DQS_A_N0_AK2 SA_DQS_8
 M_DQS_A_N1_AK3 SA_DQS_9
 M_DQS_A_N2_AK4 SA_DQS_10
 M_DQS_A_N3_AK5 SA_DQS_11
 M_DQS_A_N4_AK6 SA_DQS_12
 M_DQS_A_N5_AK7 SA_DQS_13
 M_DQS_A_N6_AK8 SA_DQS_14
 M_DQS_A_N7_AK9 SA_DQS_15

SA_WE#
 SA_CAS#
 SA_RAS#

SA_BS_0
 SA_BS_1
 SA_BS_2

SA_CSM_0
 SA_CSM_1
 SA_CSM_2
 SA_CSM_3

SA_CKE_0
 SA_CKE_1
 SA_CKE_2
 SA_CKE_3

SA_ODT_0
 SA_ODT_1
 SA_ODT_2
 SA_ODT_3

SA_CK_0
 SA_CK_1
 SA_CK_2
 SA_CK_3

SM_DRAMRST#

SA_DQS_8
 SA_DQS_8

SA_ECC_CB_0
 SA_ECC_CB_1
 SA_ECC_CB_2
 SA_ECC_CB_3
 SA_ECC_CB_4
 SA_ECC_CB_5
 SA_ECC_CB_6
 SA_ECC_CB_7

DDR_0
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DDR3 CH.A

SKT_H2_C8B

Pay Attention to This Part!

CPUD

M_DATA_B0_AG7 SB_DQ_0
 M_DATA_B1_AG8 SB_DQ_1
 M_DATA_B2_AG9 SB_DQ_2
 M_DATA_B3_AJ0 SB_DQ_3
 M_DATA_B4_AJ1 SB_DQ_4
 M_DATA_B5_AJ2 SB_DQ_5
 M_DATA_B6_AJ3 SB_DQ_6
 M_DATA_B7_AJ4 SB_DQ_7
 M_DATA_B8_AJ5 SB_DQ_8
 M_DATA_B9_AJ6 SB_DQ_9
 M_DATA_B10_AJ7 SB_DQ_10
 M_DATA_B11_AJ8 SB_DQ_11
 M_DATA_B12_AJ9 SB_DQ_12
 M_DATA_B13_AJ0 SB_DQ_13
 M_DATA_B14_AJ1 SB_DQ_14
 M_DATA_B15_AJ2 SB_DQ_15
 M_DATA_B16_AJ3 SB_DQ_16
 M_DATA_B17_AJ4 SB_DQ_17
 M_DATA_B18_AJ5 SB_DQ_18
 M_DATA_B19_AJ6 SB_DQ_19
 M_DATA_B20_AJ7 SB_DQ_20
 M_DATA_B21_AJ8 SB_DQ_21
 M_DATA_B22_AJ9 SB_DQ_22
 M_DATA_B23_AJ0 SB_DQ_23
 M_DATA_B24_AJ1 SB_DQ_24
 M_DATA_B25_AJ2 SB_DQ_25
 M_DATA_B26_AJ3 SB_DQ_26
 M_DATA_B27_AJ4 SB_DQ_27
 M_DATA_B28_AJ5 SB_DQ_28
 M_DATA_B29_AJ6 SB_DQ_29
 M_DATA_B30_AJ7 SB_DQ_30
 M_DATA_B31_AJ8 SB_DQ_31
 M_DATA_B32_AJ9 SB_DQ_32
 M_DATA_B33_AJ0 SB_DQ_33
 M_DATA_B34_AJ1 SB_DQ_34
 M_DATA_B35_AJ2 SB_DQ_35
 M_DATA_B36_AJ3 SB_DQ_36
 M_DATA_B37_AJ4 SB_DQ_37
 M_DATA_B38_AJ5 SB_DQ_38
 M_DATA_B39_AJ6 SB_DQ_39
 M_DATA_B40_AJ7 SB_DQ_40
 M_DATA_B41_AJ8 SB_DQ_41
 M_DATA_B42_AJ9 SB_DQ_42
 M_DATA_B43_AJ0 SB_DQ_43
 M_DATA_B44_AJ1 SB_DQ_44
 M_DATA_B45_AJ2 SB_DQ_45
 M_DATA_B46_AJ3 SB_DQ_46
 M_DATA_B47_AJ4 SB_DQ_47
 M_DATA_B48_AJ5 SB_DQ_48
 M_DATA_B49_AJ6 SB_DQ_49
 M_DATA_B50_AJ7 SB_DQ_50
 M_DATA_B51_AJ8 SB_DQ_51
 M_DATA_B52_AJ9 SB_DQ_52
 M_DATA_B53_AJ0 SB_DQ_53
 M_DATA_B54_AJ1 SB_DQ_54
 M_DATA_B55_AJ2 SB_DQ_55
 M_DATA_B56_AJ3 SB_DQ_56
 M_DATA_B57_AJ4 SB_DQ_57
 M_DATA_B58_AJ5 SB_DQ_58
 M_DATA_B59_AJ6 SB_DQ_59
 M_DATA_B60_AJ7 SB_DQ_60
 M_DATA_B61_AJ8 SB_DQ_61
 M_DATA_B62_AJ9 SB_DQ_62
 M_DATA_B63_AJ0 SB_DQ_63

M_DQS_B_P0_AH7 SB_DQS_0
 M_DQS_B_P1_AH8 SB_DQS_1
 M_DQS_B_P2_AH9 SB_DQS_2
 M_DQS_B_P3_AJ0 SB_DQS_3
 M_DQS_B_P4_AJ1 SB_DQS_4
 M_DQS_B_P5_AJ2 SB_DQS_5
 M_DQS_B_P6_AJ3 SB_DQS_6
 M_DQS_B_P7_AJ4 SB_DQS_7

M_DQS_B_N0_AH6 SB_DQS_8
 M_DQS_B_N1_AH7 SB_DQS_9
 M_DQS_B_N2_AH8 SB_DQS_10
 M_DQS_B_N3_AH9 SB_DQS_11
 M_DQS_B_N4_AJ0 SB_DQS_12
 M_DQS_B_N5_AJ1 SB_DQS_13
 M_DQS_B_N6_AJ2 SB_DQS_14
 M_DQS_B_N7_AJ3 SB_DQS_15

SA_CK0#
 SA_CK1#
 SA_CK2#
 SA_CK3#

SA_ODT0#
 SA_ODT1#
 SA_ODT2#
 SA_ODT3#

SA_CK0_0
 SA_CK0_1
 SA_CK0_2
 SA_CK0_3

SA_CK1_0
 SA_CK1_1
 SA_CK1_2
 SA_CK1_3

SA_CK2_0
 SA_CK2_1
 SA_CK2_2
 SA_CK2_3

SA_CK3_0
 SA_CK3_1
 SA_CK3_2
 SA_CK3_3

SB_DQS_8
 SB_DQS_8

SB_ECC_CB_0
 SB_ECC_CB_1
 SB_ECC_CB_2
 SB_ECC_CB_3
 SB_ECC_CB_4
 SB_ECC_CB_5
 SB_ECC_CB_6
 SB_ECC_CB_7

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DDR3 CH.B

SKT_H2_C8B

Elitegroup Computer Systems

CPU - DDR3

H67H2-M3

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VCC0	VR_EN	VR_EN	OVCC
VCCORE	VR_ALERT	VR_ALERT	OVCCORE
V_CPU0	VR_DATAOUT	VR_DATAOUT	OV_CCPU0
12V_4P	VR_VDD1	VR_VDD1	OV_12V_4P
VCCIN	VR_VDD2	VR_VDD2	OV_VCCIN
VIN	VR_VDD3	VR_VDD3	OV_VIN
SVSS0	VR_VSS0	VR_VSS0	OSVSS0

0	VR_SVID_ALERT1	VR_SVID_ALERT1	VR_SVID_ALERT1
0	VR_SVID_DATAOUT1	VR_SVID_DATAOUT1	VR_SVID_DATAOUT1
4	VR_SVID_CHK	VR_SVID_CHK	VR_SVID_CHK
10	VR_SVID_PWM1	VR_SVID_PWM1	VR_SVID_PWM1
10	AUI_SENP1	AUI_SENP1	AUI_VSDIOT
10	AUI_SENN1	AUI_SENN1	AUI_SENN1
10	AUI_SENP2	AUI_SENP2	AUI_SENP2
10	AUI_SENN2	AUI_SENN2	AUI_SENN2
10	AUI_SENP3	AUI_SENP3	AUI_SENP3
10	AUI_SENN3	AUI_SENN3	AUI_SENN3
10	AUI_SENP4	AUI_SENP4	AUI_SENP4
10	AUI_SENN4	AUI_SENN4	AUI_SENN4
10	VCC_SEN4	VCC_SEN4	VCC_SEN4
10	VSS_SEN4	VSS_SEN4	VSS_SEN4
4/6	VR_READY	VR_READY	VR_READY
10	AUI_PWM1	AUI_PWM1	AUI_PWM1
10	AUI_SENP1	AUI_SENP1	AUI_SENP1
10	AUI_SENN1	AUI_SENN1	AUI_SENN1
4	VCC4G_SEN	VCC4G_SEN	VCC4G_SEN
10	VSS4G_SEN	VSS4G_SEN	VSS4G_SEN

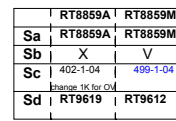
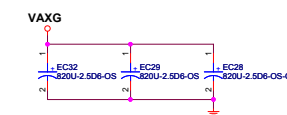
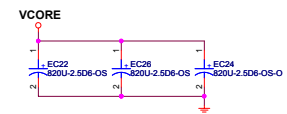
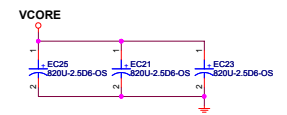
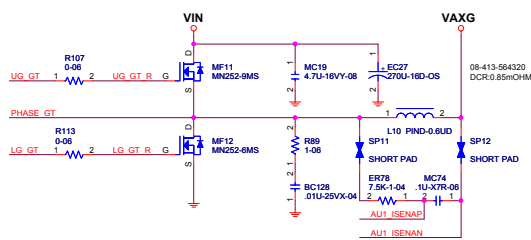
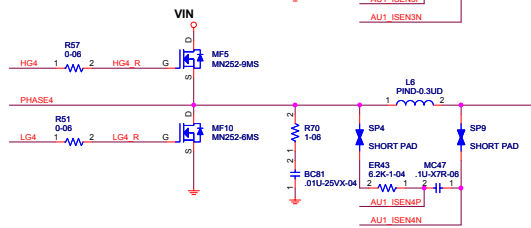
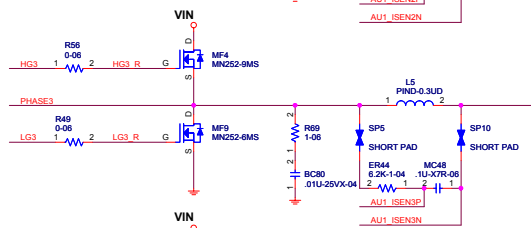
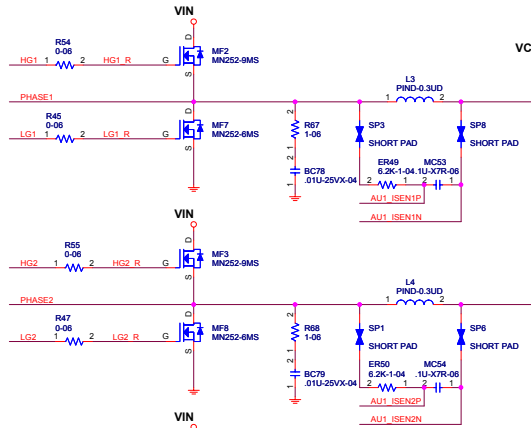
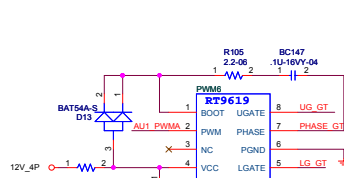
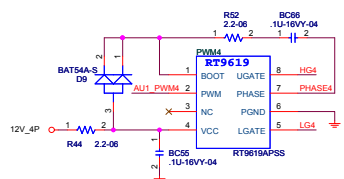
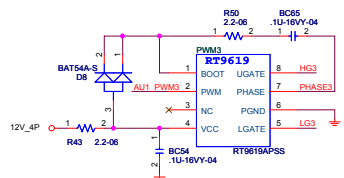
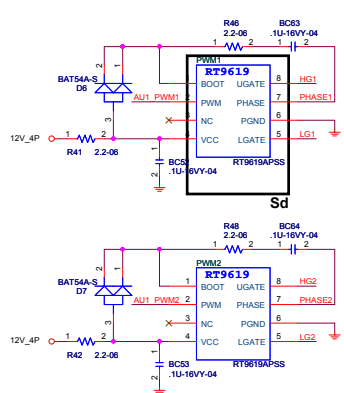


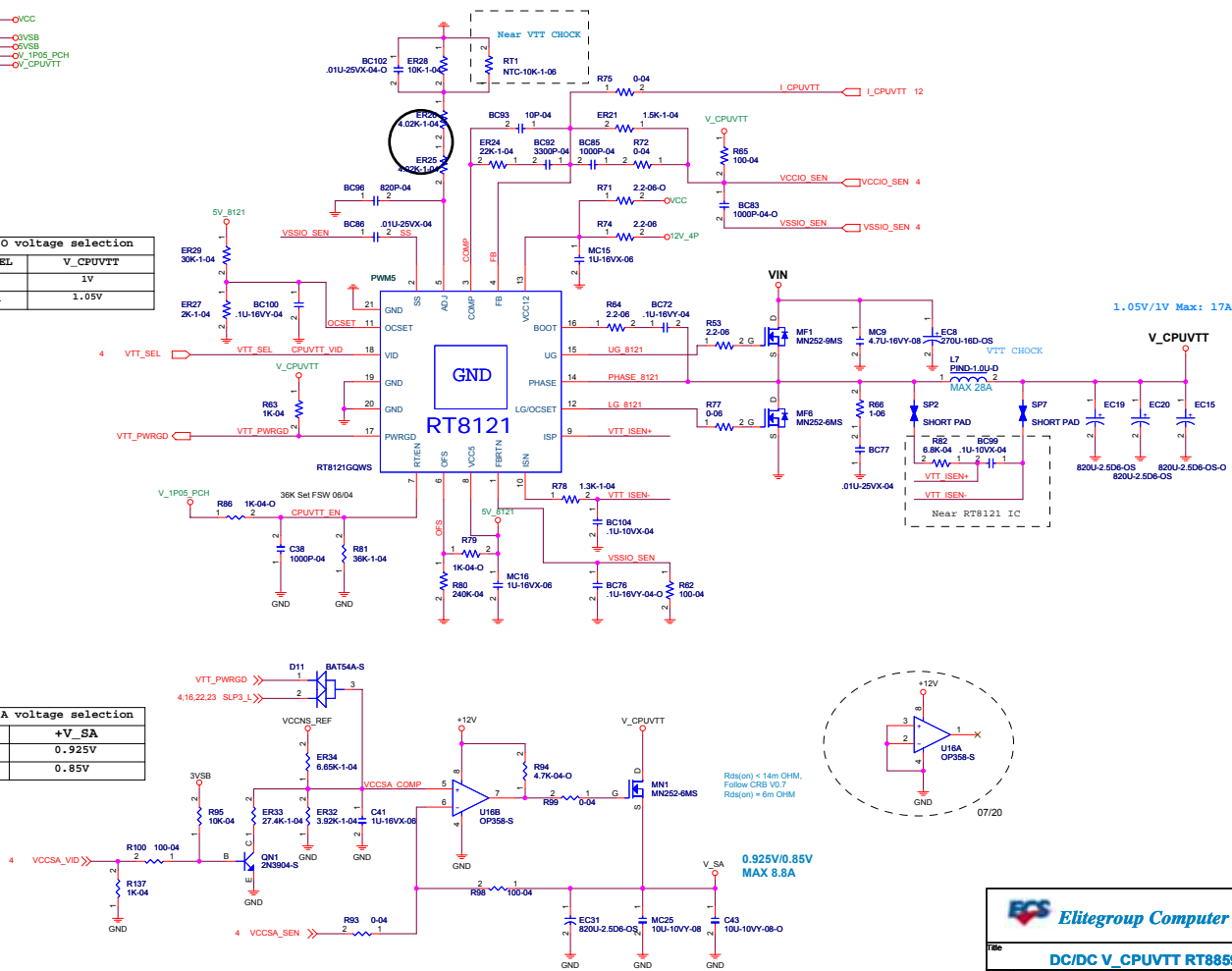
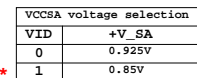
Diagram showing the pin connections for the ADXL345 module:

- VCC (Pin 1) to OVCC (Pin 16)
- VCORE (Pin 2) to VCORE (Pin 15)
- 12V 4P (Pin 3) to 12V 4P (Pin 14)
- VCC3 (Pin 4) to VCC3 (Pin 13)
- VIN (Pin 5) to VIN (Pin 12)
- AU1_PWM[1..4] (Pin 9) to AU1_PWM[1..4] (Pin 10)
- AU1_ISEN1P (Pin 9) to AU1_ISEN1P (Pin 10)
- AU1_ISEN1N (Pin 9) to AU1_ISEN1N (Pin 10)
- AU1_ISEN2P (Pin 9) to AU1_ISEN2P (Pin 10)
- AU1_ISEN2N (Pin 9) to AU1_ISEN2N (Pin 10)
- AU1_ISEN3P (Pin 9) to AU1_ISEN3P (Pin 10)
- AU1_ISEN3N (Pin 9) to AU1_ISEN3N (Pin 10)
- AU1_ISEN4P (Pin 9) to AU1_ISEN4P (Pin 10)
- AU1_ISEN4N (Pin 9) to AU1_ISEN4N (Pin 10)
- VCC_SEN (Pin 4,9) to VCC_SEN (Pin 15)
- VSS_SEN (Pin 4,9) to VSS_SEN (Pin 15)

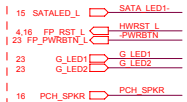


The diagram shows the 5V pin of the ATmega328P connected to the VCC pin of the ATmega328P. The connection is made using a single wire.

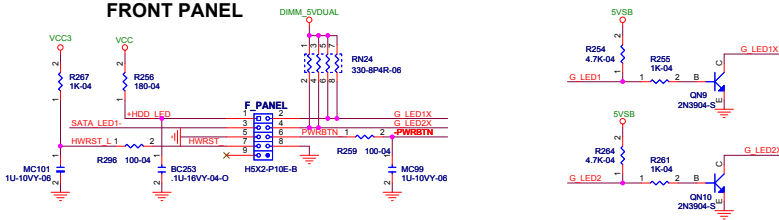
VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V



External Connection

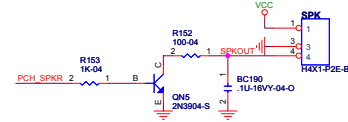


FRONT PANEL



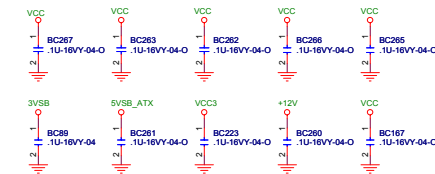
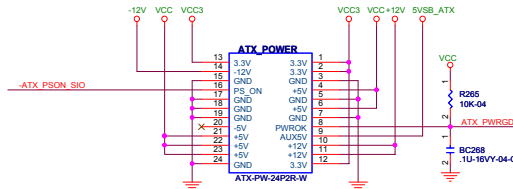
	D0	D1	D3	D4	D5
G_LED1	L	B	B	L	L
G_LED2	B	B	L	L	L
G_LED3	B	B	L	L	L
G_LED4	B	B	L	L	L
G_LED5	B	B	L	L	L

B:1111001ing



POWER CONNECTOR

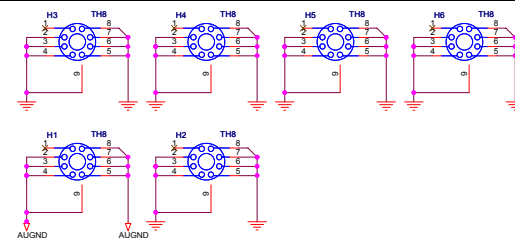
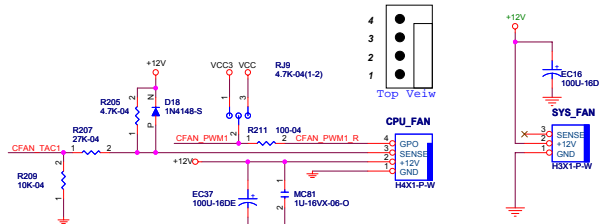
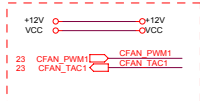
External Connection



For EMI.

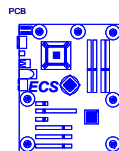
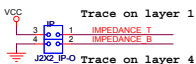
FAN

External Connection

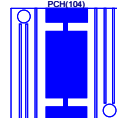


1)Circuit type 1

Layer 1:TOP
 Layer 2:PWR
 Layer 3:GND
 Layer 4:BOTTOM



PCB STACK: L1:TOP
 L2:PWR
 L3:GND
 L4:BOTTOM

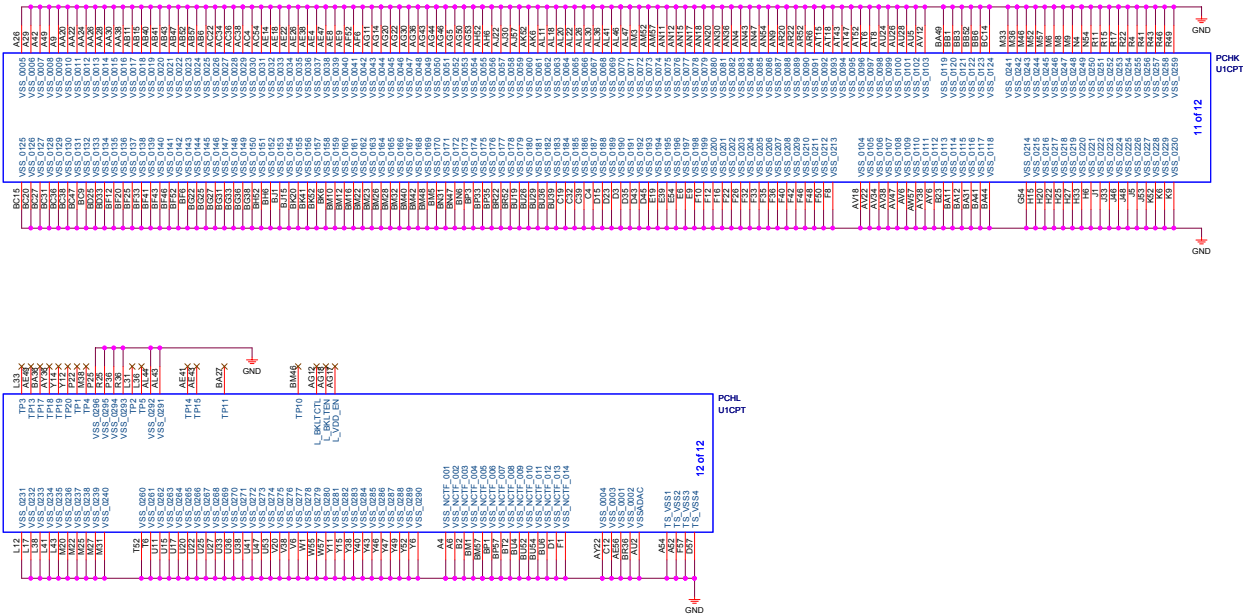



20-120-011476
 Series PN:20-120-010851

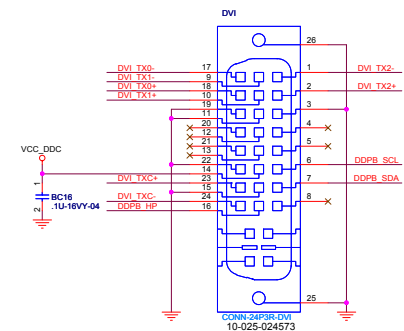


Elitegroup Computer Systems
 Front Panel,FAN,PowerConn,GND,104
 H67H2-M3
 Monday, October 11, 2010



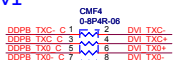


			
<i>Elitegroup Computer Systems</i>			
Title			
Slot - PCI-EX16/PCI-EX1			
Size	Document Number	Rev	
Custom	H67H2-M3	1.0	
Date:	Monday, October 11, 2010	Sheet	20 of 32

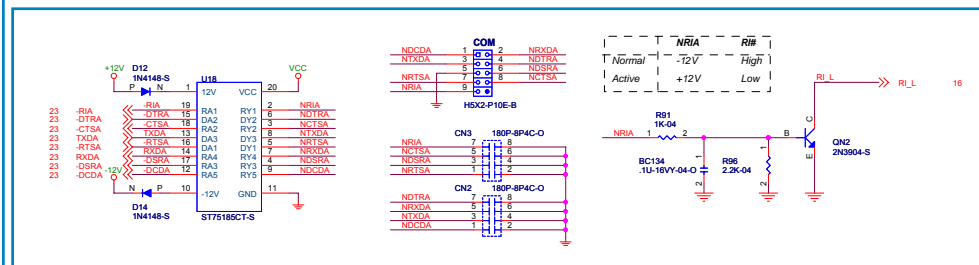
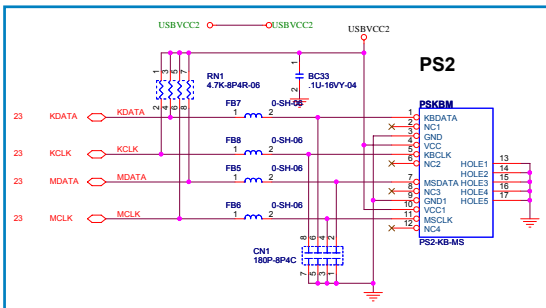
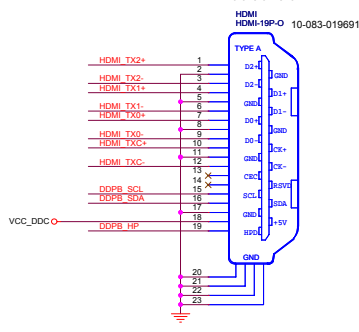
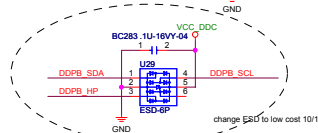
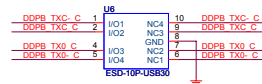
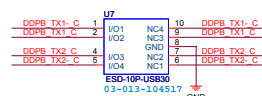
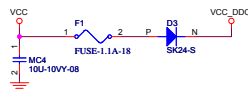


change DVI or HDMI must change GPIO in page15

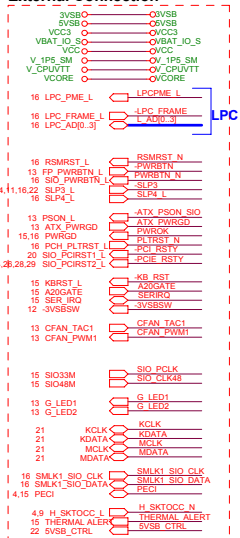
DVI



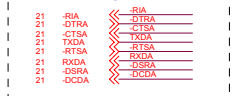
HDMI



External Connection

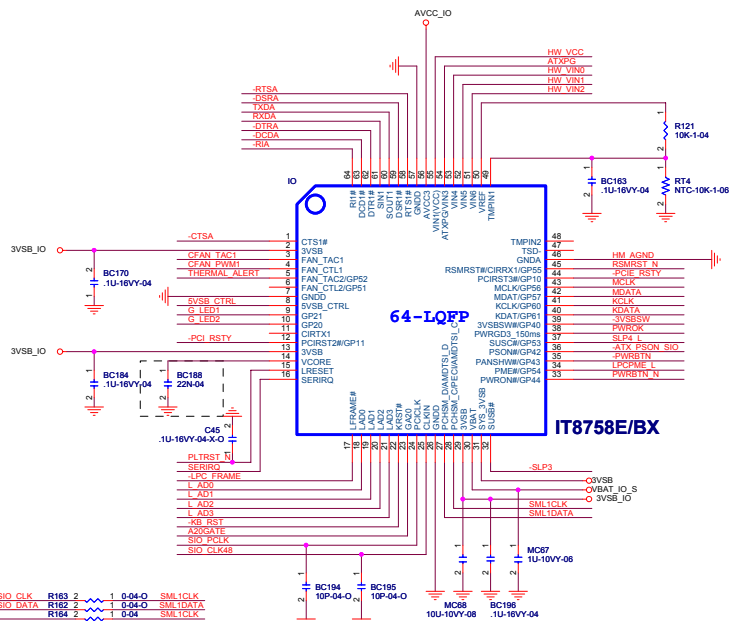


COM

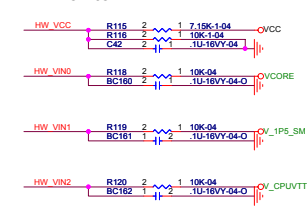


IT8758 Power On Strapping Options

FJP1 & FJP2	FAN_CTL_SEL	11	The default value of EC Index 63h/6Bh/73h is 80h (50%)
FJP2	FAN_CTL_SEL	10	The default value of EC Index 63h/6Bh/73h is FFh (Fan off)
FJP1 & FJP2	Pin 60& 23	01	The default value of EC Index 63h/6Bh/73h is 00h (Fan full speed)
FJP1 & FJP2	Pin 60& 23	00	The default value of EC Index 63h/6Bh/73h is 40h

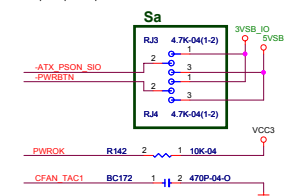


H/W Monitor



LPC Pull-ups

Note:
Most pull-ups are provided



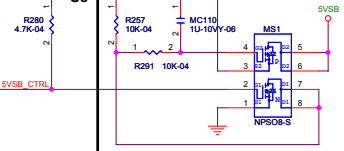
Sb



EUP

	W/O EUP	W EUP
Sa	2-3	1-2
Sb	V	X
Sc	X	V
Sd	X	V

Sc



Elitegroup Computer Systems

Model: **SIO-ITE8758E**

Document Number: **H67H2-M3**

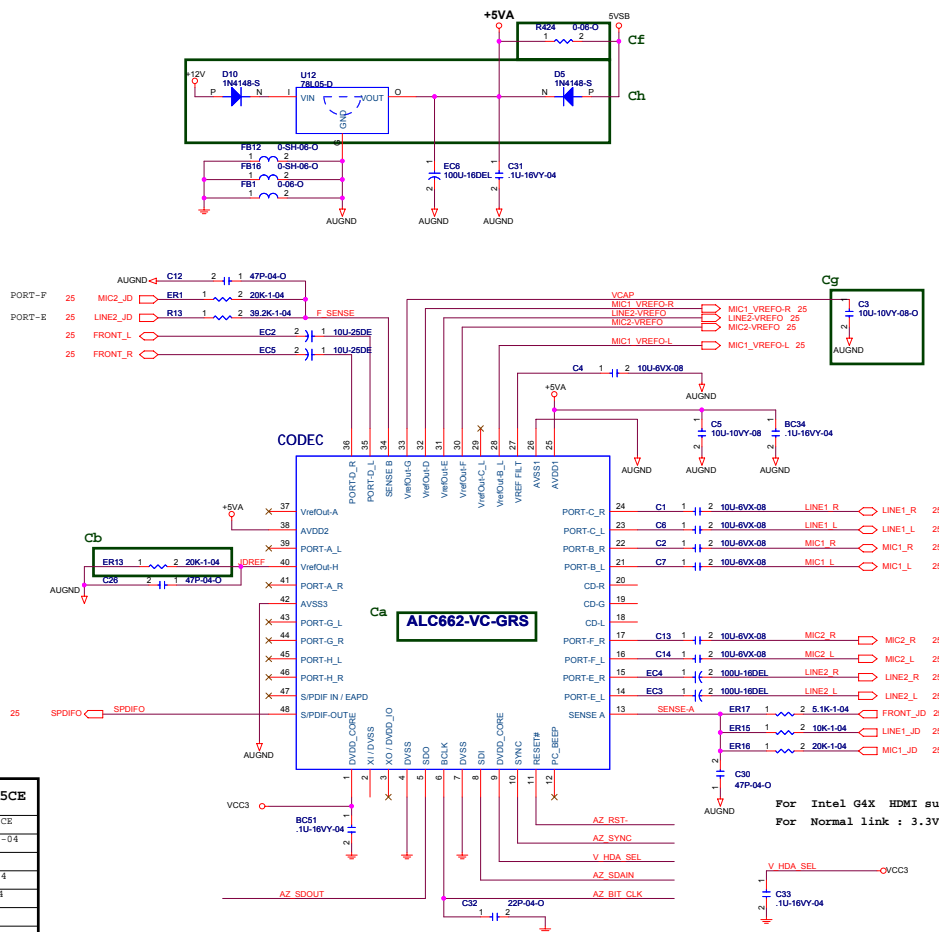
Date: Monday, October 11, 2010

Sheet: 23 of 32

External Connection



* VCC1.5 can remove for non-Intel G4X platform



BOM Difference

Location	ALC662	VT1705	VT1705CE
Ca	ALC662-VC-GRS	VT1705	VT1705CE
Cb	20K-1-04	5.1K-1-04	5.1K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	75-04	75-04
Cf	X	X	V
Cg	X	X	V
Ch	V	V	X

When you change BOM, remember change GP1 to inform BIOS use different Ver-Table.

Elitegroup Computer Systems

File

AUDIO VT1705/ALC662 (CHIP)

Site Custom

Document Number

H67H2-M3

Date: Monday, October 11, 2010

Sheet 24 of 32

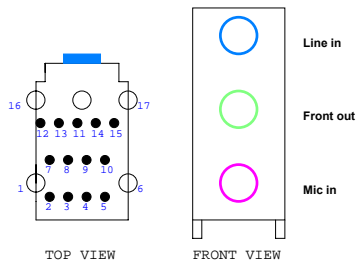
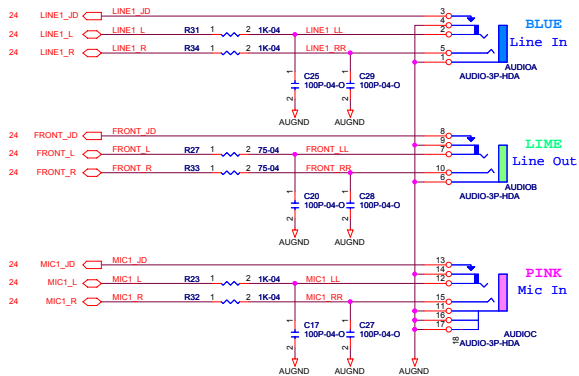
Rev 1.0

External Connection

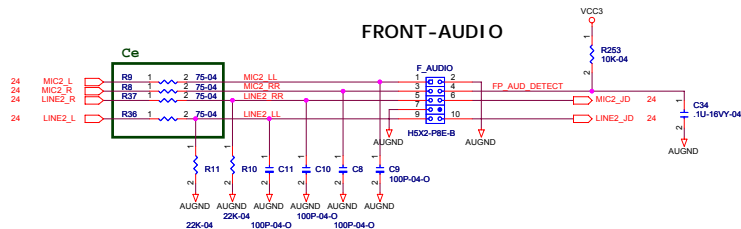
16 FP_AUD_DETECT ← FP_AUD_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

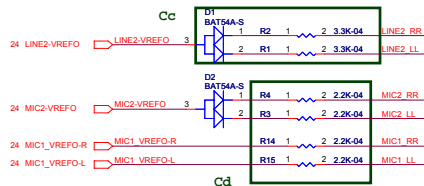
REAR-AUDIO Non re-tasking for rear panel



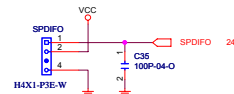
FRONT-AUDIO



MIC Bias



SPDIF-OUT

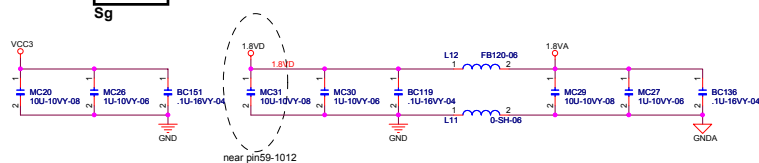
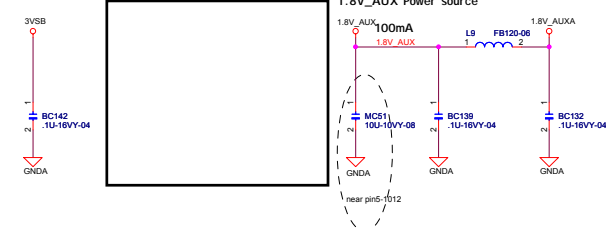
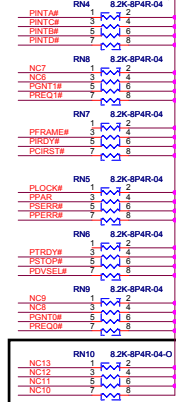
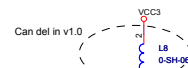
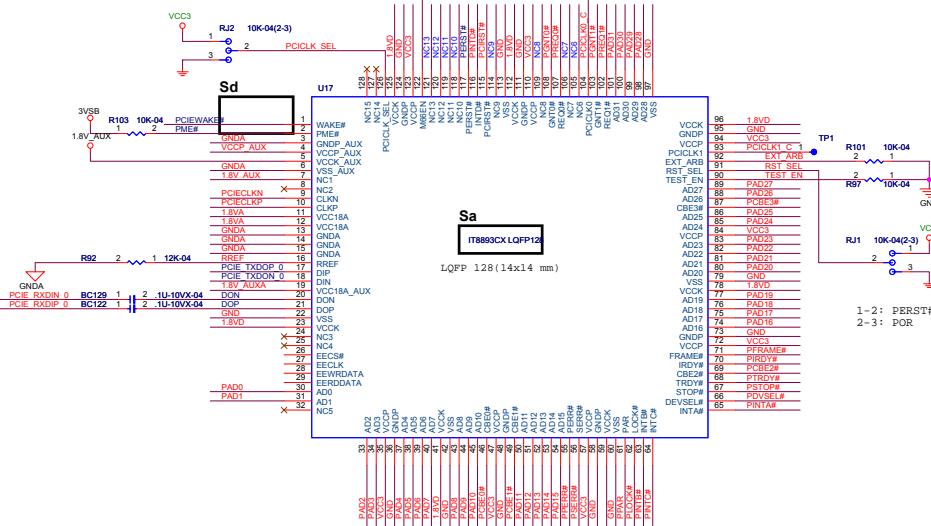
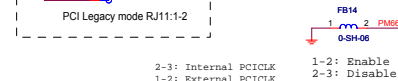
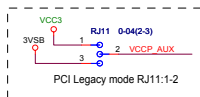


External Connection

The diagram illustrates the external connections for the VMEC-1000. It shows a VMEC-1000 module (represented by a rectangle with pins) connected to an external circuit. The connections are as follows:

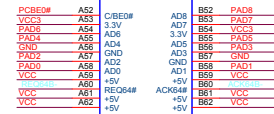
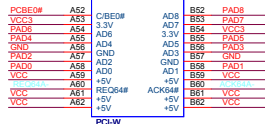
- V_IP8_SFR** (pin 1) is connected to **OV_IP8_SFR** (pin 2).
- 3VSB** (pin 3) is connected to **OV3VSB** (pin 4).
- PCIE_WAKE_1#** (pin 5) is connected to **PCIEWAKE#** (pin 6).
- PCIE_TX_P** (pin 7) is connected to **PCIE_TXDOP_0** (pin 8).
- PCIE_TX_N** (pin 9) is connected to **PCIE_TXDON_0** (pin 10).
- CK_PPE_100M_PCL_1** (pin 11) is connected to **PCIECLKP** (pin 12).
- CK_PPE_100M_PCL_1** (pin 13) is connected to **PCIECLKN** (pin 14).
- PCIE_RXD_P** (pin 15) is connected to **PCIE_RXDOP_0** (pin 16).
- PCIE_RX_N** (pin 17) is connected to **PCIE_RXDON_0** (pin 18).
- SIO_P0IRST2_L** (pin 19) is connected to **PERST#** (pin 20).

	PAD[31:0]	PAD[31:0]
27	PAGEB#	PCBE0B
	PCBE1#	PCBE1B
	PCBE2#	PCBE2B
	PCBE3#	PCBE3B
	PME#	PMEB
	PMENB	PMENB
	PFRAMB	PFRAAMB
	PREV#	PREVB
	PRDY#	PRDVB
	PSTOP#	PSTOPB
	DPOVSLEH	DPOVSLEH
	PSAR	PSARB
	PSERR#	PSERRB
	PPERR#	PPERRB
	PURST#	PCURSTB
	PLCKCH	PLCKCHB
	PLICLK1	PLICLK1B
	PINTA#	PINTAB
	PINTB#	PINTBB
	PINTC#	PINTCB
	PINTD#	PINTDB
	PRECQ#	PRECQB
	PONTOW#	PONTOWB
	PREO1#	PREO1B
28	PONT1#	PONT1B



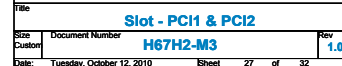
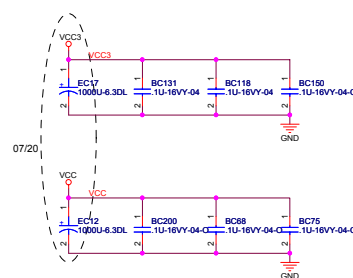
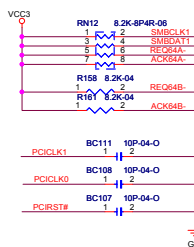
	IT8893AX	IT8893BX
Sa	IT8893AX	IT8893BX
Sb	V	X
Sc	V	X
Sd	X	V
Se	0-04(1-2)	0-04(2-3)
Sf	X	V
Sg	V	X

✓ Add PCI2 Jack 05/13



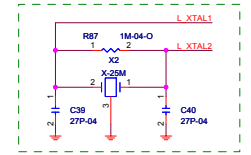
For ITE chipset auto power-on issue.

As document WW32 2010 Sandy Bridge and Cougar Point
Based Platforms Field Message of the Week



Pinout diagram for the USB-C connector of the Raspberry Pi 4. The diagram shows a 24-pin connector with pins numbered 1 to 24. Pins 1, 2, 3, and 4 are labeled USBVCC, GND, USBVCC, and GND respectively. Pins 5, 6, 7, and 8 are labeled 3V5B0, GND, 0V5B0, and GND. Pins 9, 10, 11, and 12 are labeled VCC3, GND, VCC3, and GND. Pins 13, 14, 15, and 16 are labeled AUGND2, GND, AUGND2, and GND. Pins 17, 18, 19, and 20 are labeled PCIE_WAKE_L, PCIE_WAKE_UP, PCIE_LAN1_RST, and PCIE_LAN1_RST. Pins 21, 22, 23, and 24 are labeled CK_LANE1_H, CK_LANE1_H, CK_LANE1_L, and CK_LANE1_L. Pins 25, 26, 27, and 28 are labeled LAN_TX_P, LAN_TX_N, LAN_RX_P, and LAN_RX_N. Pins 29, 30, 31, and 32 are labeled LAN_TX_P, LAN_TX_N, LAN_RX_P, and LAN_RX_N. Pins 33, 34, 35, and 36 are labeled USB_N10, USB_P10, USB_N11, and USB_P11. Pins 37, 38, 39, and 40 are labeled USB_N10, USB_P10, USB_N11, and USB_P11.

29	U1_RP0	LSRX0+
29	U1_RN0	LSRX0-
29	U1_RP1	LSRX1+
29	U1_RN1	LSRX1-
29	U1TP0	LSTX0+
29	U1TN0	LSTX0-
29	U1TP1	LSTX1+
29	U1TN1	LSTX1-
29	U2IC_P0	U2IC P0
29	U2IC_N0	U2IC N0
29	U2IC_P1	U2IC P1
29	U2IC_N1	U2IC N1



VDD1.05_A

Closed To Pin6,9,41

BC84 1 2 .1U-18VY-04

BC91 1 2 .1U-18VY-04

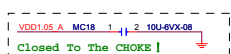
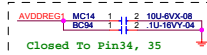
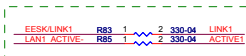
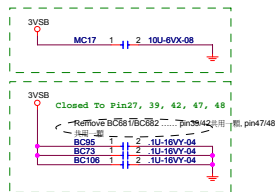
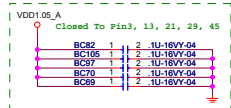
3V3B

Closed To Pin12

BC74 1 2 .1U-18VY-04

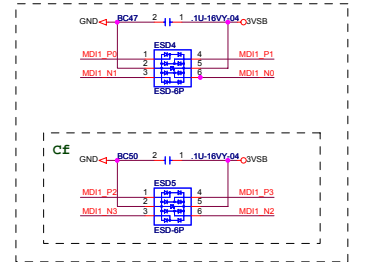
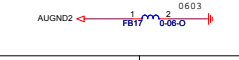
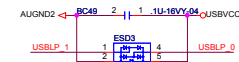
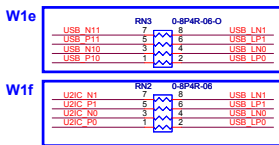
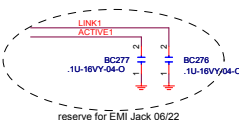
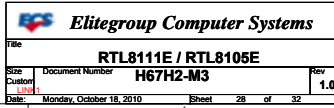
	RTL8111E-GR 1000M	RTL8105E-GR 10/100M
Ca	RTL8111E-VB-GR	RTL8105E-GR
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-25VX-04
Cf	V	X
Cg		

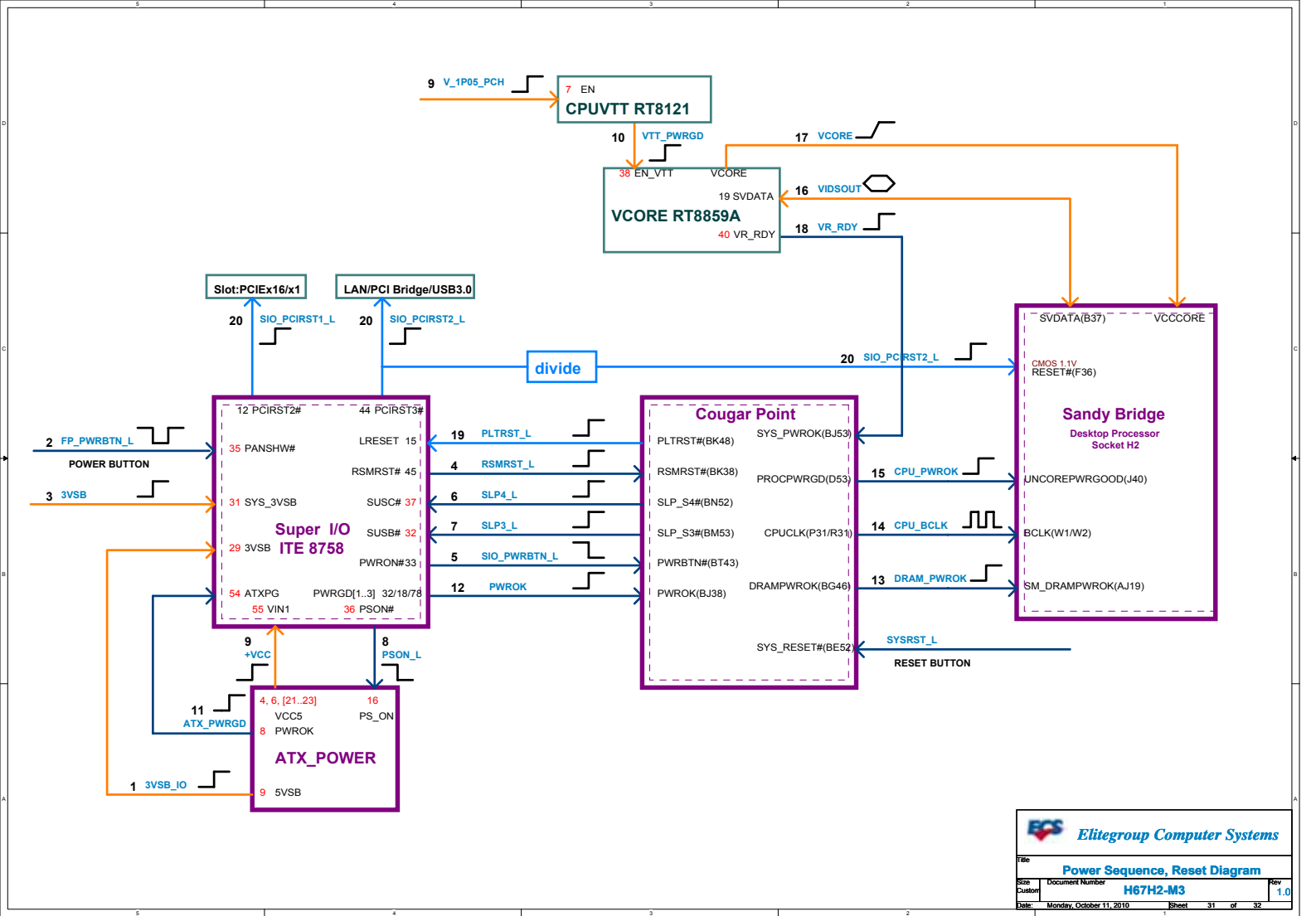
LAN_HSOP/N請接到SB的PCIE RX端
LAN_HSIP/N請接到SB的PCIE TX端
LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

[illegible]

The schematic diagram illustrates the power plane for the Intel Atom D4250. It shows the following connections and components:

- AVDDOUT1** and **AVDDREG1** are connected to the **3V5S** rail.
- EEDP/SDA1** and **EECS/SCL1** are connected to the **3V5S** rail.
- PCIE WAKE UP-** is connected to the **3V5S** rail.
- LAN1_ISO** and **PCIE LAN1_RST-** are connected to the **VCC3** rail.
- Inductors (L2, FB13, R76, R73, R58, R61)** are placed between the power rails and the components.
- Capacitors (IND-4.7U-S, 10K-04, 1K-04, 15K-04)** are used for decoupling and filtering.

[illegible]



NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

